REMARKS

I. Introduction

In response to the Office Action dated November 3, 2006, Applicants have amended claim 1, canceled claims 2 – 5 and 7 – 9, and added new claim 18. Care has been taken to avoid the introduction of new matter. In view of the foregoing amendments and the following remarks, Applicants respectfully submit that all pending claims are in condition for allowance.

II. Election/Restriction

In response to the restriction requirement, Applicants elected Species III, Embodiment 3, Figure 3, and identified claims 1, 5, and 11 – 14 as reading on the elected species. Upon further consideration, Applicants recognized that claims 15 and 16 are also readable on this embodiment. Accordingly, Applicants respectfully request that the Examiner consider claims 15 and 16 in the next office correspondence.

III. Double Patenting Rejections

Claims 1, 5, and 11 – 14 have been provisionally rejected on the ground of non-statutory obviousness-type double patenting as allegedly being unpatentable over claims 1, 5, 13, and 18 – 20 of co-pending Patent Application No. 10/913,356. Applicants submit herewith a terminal disclaimer so as to overcome this rejection.

IV. Claims Rejections Under 35 U.S.C. §§ 102 and 103

Claims 1 and 14 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 6,920,026 to Chen. Claims 5 and 11 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Chen in view of U.S. Patent No. 6,552,886 to Wu. Claims 12

and 13 stand rejected under § 103 as allegedly being unpatentable over Chen in view of U.S. Patent No. 6,437,407 to Ker. Applicants traverse these rejections for at least the following reasons.

Claim 1 recites, among other thing, a semiconductor integrated circuit comprising an inter-power supply electrostatic discharge protection circuit which comprises a first gate voltage control circuit capable of controlling the gate voltage of the gate insulating element, wherein the gate insulating element is a first NMIS transistor whose source is connected to the ground line and whose drain is connected to the power supply line and the first gate voltage control circuit comprises: a first Schmidt trigger circuit connected at its output to the gate of the first NMIS transistor; a resistor whose one end is connected to the power supply line and whose other end is connected to an input of the first Schmidt trigger circuit; and a capacitor whose one end is connected to the ground line and whose other end is connected to the input of the first Schmidt trigger circuit.

Chen discloses an ESD detection circuit which comprises an NMOS transistor Mn8 having a source electrode connected to a ground line VSS and a drain electrode connected to a power supply line VDD, a capacitor C6 whose one end is connected to the power supply line VDD and whose other end is connected to a gate electrode of the NMOS transistor Mn8, and a resistor R7 whose one end is connected to the ground line VSS and whose other end is connected to the gate electrode NMOS transistor Mn8. Chen does not disclose or even suggest the use of a Schmidt trigger circuit, as recited in claim 1. Furthermore, the arrangement of the capacitor and resistor as taught by Chen is opposite to the placement recited in claim 1.

Wu does not overcome the deficiencies of Chen. Wu discloses a hysteresis transistor 28 comprising inverters 32, 33, and 34, and a p-channel transistor. Even if the circuit having the

hysteresis transistor 28 is applied to the circuit disclosed by Chen, the combination of Wu and Chen still fail to disclose the arrangement of the capacitor and resistor and the use of a Schmidt trigger as recited in claim 1.

Thus, as each and every limitation must be disclosed or suggested by the prior art references in order to establish a *prima facie* case of obviousness (MPEP § 2143.03), and Wu and Chen, alone or in combination with each other, fail to disclose or suggest at least the features recited above, it is respectfully submitted that independent claim 1 is patentable over the cited reference.

Claims 11 – 16 and 18 depend from claim 1. Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Harness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as the independent claims are patentable for at least the reasons set forth above, it is respectfully submitted that all dependent claims are also in condition for allowance. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

V. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:DAB
Facsimile: 202.756.8087
Date: January 23, 2007